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(54) **Title: METHOD AND APPARATUS FOR PLATING AND POLISHING A SEMICONDUCTOR SUBSTRATE**
(54) **Titre: PROCEDE ET APPAREIL DE REVETEMENT ET DE POLISSAGE D'UN SUBSTRAT SEMICONDUCTEUR**

(57) Abstract

The present invention provides a method and apparatus that plates/deposits a conductive material on a semiconductor substrate (2) and then polishes the same substrate (2). This is achieved by providing multiple chambers (100, 200) in a single apparatus, where one chamber (100) can be used for plating/depositing the conductive material and another chamber (200) can be used for polishing the semiconductor substrate. The plating/depositing process can be performed using brush plating or electrochemical mechanical deposition and the polishing process can be performed using electropolishing or chemical mechanical polishing. The present invention further provides a method and apparatus for intermittently applying the conductive material to the semiconductor substrate (2) and also intermittently polishing the substrate (2) when such conductive material is not being applied to the substrate (2). Furthermore, the present invention provides a method and apparatus that plates/deposits and/or polishes a conductive material and improves the electrolyte mass transfer properties on a substrate (2) using a novel anode assembly.

(57) Abrégé

La présente invention concerne un procédé et un appareil permettant de réaliser un revêtement/dépôt de matériau conducteur sur un substrat (2) semiconducteur, puis de polir ledit substrat (2). A cet effet, on utilise un seul appareil comportant plusieurs chambres (100, 200), une chambre (100) pouvant être utilisée pour le revêtement /dépôt de matériau conducteur, une autre chambre (200) pouvant être utilisée pour le polissage du substrat semiconducteur. Le procédé de revêtement /dépôt peut être réalisé par dépôt à la brosse ou dépôt mécanique électrochimique, et le procédé de polissage peut être réalisé par électropolissage ou polissage mécanique chimique. La présente invention concerne également un procédé et un appareil permettant d'appliquer par intermittence le matériau conducteur sur le substrat (2) semiconducteur, et de polir également par intermittence ledit substrat (2) lorsque le matériau conducteur n'est pas en train d'être appliqué sur le substrat (2). En outre, la présente invention concerne un procédé et un appareil permettant de réaliser un revêtement/dépôt et/ou de procéder au polissage d'un matériau conducteur, tout en améliorant les propriétés de transfert de masse de l'électrolyte sur le substrat (2) par l'utilisation d'un nouvel ensemble d'anode.

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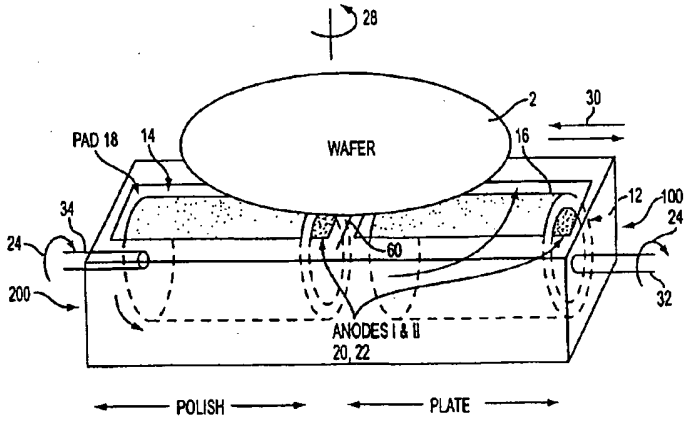

(57) Abstract

The present invention provides a method and apparatus that plates/deposits a conductive material on a semiconductor substrate (2) and then polishes the same substrate (2). This is achieved by providing multiple chambers (100, 200) in a single apparatus, where one chamber (100) can be used for plating/depositing the conductive material and another chamber (200) can be used for polishing the semiconductor substrate. The plating/depositing process can be performed using brush plating or electrochemical mechanical deposition and the polishing process can be performed using electropolishing or chemical mechanical polishing. The present invention further provides a method and apparatus for intermittently applying the conductive material to the semiconductor substrate (2) and also intermittently polishing the substrate (2) when such conductive material is not being applied to the substrate (2). Furthermore, the present invention provides a method and apparatus that plates/deposits and/or polishes a conductive material and improves the electrolyte mass transfer properties on a substrate (2) using a novel anode assembly.

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METHOD AND APPARATUS FOR PLATING AND POLISHING A SEMICONDUCTOR SUBSTRATE

Field of the Invention

This invention relates to a method and apparatus for plating and polishing a conductive material on a semiconductor substrate. More particularly, the invention is directed to a method and apparatus for first plating and then polishing the conductive material on the semiconductor substrate using a single apparatus. Moreover, the invention is directed to a method and apparatus for intermittently applying the conductive material to the semiconductor substrate and also intermittently polishing the substrate when such conductive material is not being applied to the substrate. Also, the invention provides a method and apparatus that plates/deposits and/or polishes a conductive material on a substrate surface using a novel pad assembly.

Background of the Invention

A conventional process step in the manufacturing of integrated circuits and devices involves plating a metal layer on a semiconductor wafer surface using a plating apparatus. Typically, the wafer surface has been previously etched and contains many holes and/or trenches. One goal of wafer plating is to uniformly fill the holes and trenches with a conductive material. However, it is very difficult to uniformly fill the holes and trenches such that no voids exist. It is well known that the existence of the voids results in poor performance and defective devices. After such plating step, a polishing step is typically performed using a polishing apparatus to achieve a generally planar surface on the wafer.

Plating the wafer surface with the conductive material over a seed metal layer has important and broad application in the semiconductor industry. Traditionally, aluminum and other metals are plated as one of many metal layers that make up a semiconductor chip. However, in recent times, there is great interest in copper deposition for interconnects on semiconductor chips, because, compared to aluminum, copper reduces electrical resistance and allows semiconductor chips to run faster with less heat generation, resulting in a significant gain in chip capacity and efficiency. Furthermore, copper is known to be a better conductor than aluminum.

Thin film plating of copper into sub-micron holes and trenches is becoming more difficult in ULSI chip processing, particularly when the feature size is below 0.25 μm with the aspect ratio greater than 5 to 1. Common chemical vapor deposition is being used to fill these holes and trenches etched into silicon substrates. Unfortunately, this process so far has yielded a very high cost for developing and integrating interconnects for ULSI technology.

Accordingly, a more accurate, cost effective, and reliable manner of applying a conductive material to the semiconductor substrate is needed.

Summary of the Invention

It is an object of the present invention to provide a method and apparatus that plates/deposits a conductive material on a semiconductor workpiece surface and then polishes the same workpiece surface.

It is another object of the invention to provide a method and apparatus that plates/deposits a conductive material on a workpiece surface using brush plating or electrochemical mechanical deposition and polishes the same workpiece surface using electropolishing or chemical mechanical polishing.

It is a further object of the invention to provide a method and apparatus having multiple chambers in a single apparatus for plating/depositing the conductive material and polishing the workpiece surface.

It is yet another object to provide a method and apparatus having novel pad assemblies for both plating/depositing the conductive material and polishing the workpiece surface.

It is yet another object to provide a method and apparatus that plates/deposits a conductive material on a workpiece surface without a pad or other fixed feature making direct contact with the workpiece surface.

These and other object of the invention are obtained by providing separate plating and polishing steps in close proximity of each other in a single apparatus. A first chamber may be used to plate/deposit the conductive material from an electrolyte solution to the workpiece surface. This is achieved by providing a pad mounted on a cylindrical anode and applying the conductive material to the workpiece surface using the electrolyte solution disposed on the pad, or through the pad.

An apparatus that performs such plating includes an anode and a cathode, a workpiece, or a workpiece that is spaced apart from the anode. A pad mounted on the cylindrical anode rotates about a first axis and the workpiece rotates about a second axis, and metal from the electrolyte solution is deposited on the workpiece when a potential difference is applied between the workpiece and the anode.

Alternatively, the plating chamber may include an anode plate spaced apart from the cathode or the workpiece. Upon application of power to the anode plate and the cathode, the electrolyte solution disposed in the plating chamber is used to deposit the conductive material on the workpiece surface.

In a polishing chamber, a pad is also mounted on another cylindrical anode or a cylindrical roller for polishing the workpiece surface. Polishing may be accomplished using either an electro-polish or a chemical mechanical polishing method. The polishing of the workpiece surface preferably prevents accumulation of the conductive material to certain areas of the workpiece while providing a generally planar surface.

The present invention further describes novel anode assemblies having unique anode-pad arrangements that can be used to plate and/or polish the workpiece surface.

Brief Description of the Drawings

These and other objects and advantages of the invention will become apparent and more readily appreciated from the following detailed description of the presently preferred exemplary embodiment of the invention taken in conjunction with the accompanying drawings, of which:

Fig. 1 illustrates a representative via to be filled with a conductor in accordance with the invention;

Fig. 2 illustrates a perspective view of a first preferred embodiment of the invention;

Fig. 3 illustrates a cross sectional view of a first preferred embodiment of the invention;

Fig. 4 illustrates a perspective view of a second preferred embodiment of the invention;

Fig. 5 illustrates a cross sectional side view of a second preferred embodiment of the invention;

Fig. 6 illustrates a perspective view of a first novel anode assembly in accordance with the preferred embodiment of the invention;

Fig. 7 illustrates a cross sectional view of a first novel anode assembly in accordance with the preferred embodiment of the invention;.

Fig. 8 illustrates a perspective view of a second novel anode assembly in accordance with the preferred embodiment of the invention;

Fig. 9 illustrates a cross sectional view of a second novel anode assembly in accordance with the preferred embodiment of the invention;

Fig. 10 illustrates a cross sectional view of a "proximity plating" apparatus and method in accordance with the preferred embodiment of the invention;

Fig. 11 illustrates a cross sectional view of a substrate having various layers and grains disposed thereon; and.

Figs. 12A-12B illustrate cross sectional views of a method for advantageously affecting the texture of a conductive material in accordance with the preferred embodiment of the invention..

Detailed Description of the Preferred Embodiments

The preferred embodiments of the present invention will now be described with reference to Figs. 1-12. As noted above, conventional processing uses different equipment, at different times, to obtain conductive material within holes and trenches, or at other desired locations on the surface of a semiconductor wafer that contains many different semiconductor chips. Accordingly, the equipment cost needed to manufacture a high quality semiconductor integrated circuit device can be exorbitant.

The present invention contemplates different embodiments, which allow for the same apparatus, to be used to plate/deposit a conductive material onto the surface and into the contact, via holes, and trenches, as well as to polish the wafer surface. While the present invention can be used with any conductive material, it is especially suited for use with copper as the conductor, and for use in the fabrication of ULSI integrated circuits having submicron features with large aspect ratios.

Furthermore, although a semiconductor wafer will be used to describe the preferred embodiments of the present invention, other semiconductor workpieces such as a flat panel or magnetic film head may be used in accordance with the present invention.

Fig. 1 illustrates a section of a wafer 2 where a via is to be formed. The via, as known in the semiconductor arts, is a conductive material that electrically couples different circuit layers. As shown in Fig. 1, the via contains a conductor 8 that can connect a lower level conductive layer 4 with an upper level conductive layer 6, with an insulative material 10 disposed therearound. It is understood that the present invention can operate upon any metal layer of a multi-layer integrated circuit chip.

Fig. 2 illustrates a perspective view and Fig. 3 illustrates a cross sectional view of a first preferred embodiment of the present invention. Referring back to Figs. 2 - 3, a conductive material, preferably copper, is applied in vias, trenches, and/or other desired areas of a wafer using an electrolyte solution 11 from a first chamber 100, while in a second chamber 200, build-up of the conductive material on undesired areas is eliminated, or at least minimized, due to the electropolishing or chemical mechanical polishing performed on the face of the wafer, but not in the contact, via holes, and trenches. The first chamber 100 is separated from the second chamber 200 by a center partition 60.

The first and second chambers 100, 200 each include an anode assembly 12, 14 having a circular or square mechanical pad 16, 18 mounted on a cylindrical anode 20, 22 that rotates around a first axis 24, and a wafer head assembly 26 having a wafer 2 that rotates around a second axis 28. The entire wafer head assembly 26 is further adapted to move side to side in the direction of arrow 30 so that the center area of the wafer 2 can be plated and polished. The cylindrical anodes 20, 22 are connected to shafts 32, 34 for rotating about axis 24. As illustrated, the wafer 2 rotates within an area that is covered by the mechanical pads 16, 18, as will be described in further detail hereinafter, which area is within chambers 100, 200 that keeps the electrolyte solution 11 disposed therein. Although shown as operating upon a single wafer, it is understood that a plurality of wafer head assemblies 26 could be used with the present invention.

With reference to Fig. 3, the wafer head assembly 26 may include a nonconductive, preferably circular, chuck 36 with a cavity that is preferably a few millimeters deep at its center and which cavity may contain a resting pad (not shown). The wafer 2 is loaded into the cavity, backside

first, against the resting pad using a conventional type of transport or vacuum mechanism to ensure that the wafer 2 is stationary with respect to the wafer head assembly 26 while in use. A nonconductive retaining ring 40 such as an O-ring or other rubber type of seal at the periphery of the wafer head assembly 26 and a cathode contact electrode 38 each push against the edge of the wafer 2 and hold the wafer 2 in place. The entire back side of the wafer 2 which pushes against the chuck 36 that is under the retaining ring 40 is thus protected from any and all solutions, including electrolyte. Other conventional wafer head assemblies can be used in accordance with the present invention.

Instead of using the cathode contacts 38 described above, the electric potential can be applied to the wafer using a ring conductor. Further, other methods of applying the electric potential to the wafer may be used in accordance with the present invention. For example, a liquid conductor or an inflatable tube coated with a conductive material may be used in the present invention. An example of using the liquid conductor or the conductive tube to provide the necessary electric potential according to the present invention is disclosed in the co-pending U.S. Application Serial No. 09/283,024, Atty. Dkt. # 42496/0253036, entitled "Method And Apparatus For Forming an Electric Contact With a Semiconductor Substrate", commonly owned by the assignee of the present invention, the contents of which are expressly incorporated herein by reference.

In accordance with the present invention, the first chamber 100 may be used for plating and the second chamber 200 may be used for polishing. The two chambers 100, 200 can be used inter-changeably where the first chamber 100 can be used for polishing and the second chamber 200 can be used for plating. As described earlier, the first chamber 100 includes the first anode assembly 12 for plating and the second chamber 200 includes the second anode assembly 14 for electropolishing. Electric potentials are applied to the anode 20, the anode 22 and the wafer 2. Any known method for providing the electric potentials to the two cylindrical anodes can be used in the present invention. As is known in the art, the difference in the amount of electric potential applied to each of the two cylindrical anodes 20, 22 determines which anode assembly is used for plating and which one is used for electropolishing.

An electrolyte solution 11 is flowed from bottom openings 50 of the two chambers 100, 200 until the solution 11 makes contact with the pads 16, 18. The electrolyte solution 11 is further circulated via side openings 52 to channel 54 to the bottom openings 50. The electrolyte solution 11 can be originally fed into the first and second chambers 100, 200 via a reservoir (not shown) through an in-channel (not shown).

In the first chamber 100, a first electric potential difference between the cylindrical anode 20 and the cathode wafer 2 allows the metal in the electrolyte solution 11 to be plated on the wafer surface via pad 16. In the second chamber 200, polishing of the wafer is undertaken by a second electrical potential difference between the cylindrical anode 22 and the cathode wafer 2.

The plating process of the present invention can be implemented using a brush plating method or an "electrochemical mechanical deposition" method. A more detailed description of the "electrochemical mechanical deposition" method can be found in the co-pending U.S. Application Serial No. 09/201,929, titled "Method and Apparatus For Electro Chemical Mechanical Deposition", commonly owned by the assignee of the present invention, the contents of which are expressly incorporated herein by reference.

The polishing process of the present invention may be implemented by way of electro-polishing or by chemical mechanical polishing as described in more detail hereinafter. In operation, it will be appreciated that the roller-shaped mechanical pad 18 polishes the wafer similar to the manner in which a roller sander removes paints from a wall.

In the polishing chamber 200, the mechanical pad 18 can have a size that polishes a section of the wafer 2 at any given time. One or more drive assemblies (not shown) are also included to rotate the cylindrical anodes 20, 22, and thereby the mechanical pads 16, 18, so that they are in contact with the section of the wafer 2 that needs to be plated and polished. The mechanical pads 16, 18 are preferably made of a nonconductive, porous type material such as polyurethane. Also, the mechanical pads 16, 18 preferably have a circular shape, but may be shaped in any other form so long as they can effectively plate and/or polish the wafer.

Fig. 4 illustrates a perspective view and Fig. 5 illustrates a cross sectional view of a second preferred embodiment of the present invention. The second preferred embodiment is also implemented with a first chamber 300 for plating and a second chamber 400 for polishing the wafer 2. The first chamber 300 is separated from the second chamber 400 by a center partition/wall 460.

Now referring to Fig. 5, the first chamber 300 includes an anode plate 306 on the bottom of the chamber 300. Any known method for attaching the anode plate 306 or shape to the bottom of the chamber 300 may be used. The electrolyte solution 11 is circulated via drain channels 302 to the bottom opening 304, or through the anode plate 306.

The second chamber 400 includes a mechanical pad 402 mounted on a cylindrical roller 404 for chemical mechanical polishing (CMP) of the wafer 2. A shaft 406 is used to rotate the roller around axis 408. CMP is a material planarization process that combines chemical removal of semiconductor layers such as insulators or metals with mechanical buffering of the substrate surface. CMP may provide global planarization of the wafer surface. For example, during the wafer fabrication process, CMP is often used to polish the profiles that build up in multilevel metal interconnection schemes.

In operation according to the second preferred embodiment of the invention, the apparatus applies, using a power source, a negative potential to the cathode contact 38 and a positive potential to the anode plate/shade 306. When an electric current is established between the two electrodes, metal

in electrolyte is deposited on the surface of the wafer 2.

After such deposition, there is also performed a mechanical chemical polishing of the wafer 2 using the mechanical pad assembly 412. A polishing agent or slurry may be applied to the polishing pad 402 via slurry channel 410 to polish the wafer 2. A center wall 420 separating the second chamber 400 from the first chamber 300 should be sufficiently high so that the slurry does not enter the first chamber 300. Other conventional methods for preventing the slurry from entering the plating chamber 300 can be used in the present invention. The mechanical pad assembly 412 substantially prevents metals from becoming permanently deposited on surfaces of the wafer 2 where such a deposit is undesired, due to the polishing or rubbing action of the mechanical pad 402. Accordingly, metal, i.e. copper, is deposited in vias, trenches, and the like where desired, and is substantially prevented from being deposited in undesired areas such as the surface or field area on the wafer.

The wafer head assembly 26 faces toward the mechanical pad assembly 412, and is pushed down with a controlled force. The wafer head assembly 26 is similar to that described with reference to Figs. 2 and 3 and rotates around axis 28 using a conventional motorized spindle (not shown). The wafer head assembly 26 is also adapted to move side to side in the direction of arrow 30 so that the center area of the wafer 2 may be plated and polished.

The present invention may reduce the need for pulse generating power supplies because the mechanical pulsing that is generated from the movement of the pad creates sufficient pulsing. This mechanical pulsing is created as a result of the wafer being in contact with the pad as it is moved in relation to the wafer. The benefit of the mechanical pulsing is that it improves grain size and copper film integrity without the need for power supplies with pulsing capabilities.

It is noted that the scope of the present invention contemplates interchanging the plating methods and the polishing methods of the first and second preferred embodiments of the invention with each other. For example, the CMP method of the second preferred embodiment can be interchanged with the electropolishing method of the first preferred embodiment. Likewise, the plating method of the first embodiment can be interchanged with the plating method of the second embodiment.

Although only two embodiments of the invention have been described in detail, the present invention can be implemented with any number of containers using various plating and polishing methods to achieve the objects of the invention. For example, three chambers may be used in the invention where the center chamber can be used for polishing while the left and right chambers can be used for plating/depositing.

The invention as illustrated in Figs. 6-9 further describes a method and apparatus for intermittently applying the conductive material to the semiconductor substrate and also intermittently polishing the substrate when such conductive material is not being applied to the substrate. When

intermittently applying the conductive material, the present invention applies electrical current having a potential difference between the workpiece and the anode so that the conductive material can be applied to the workpiece when such current is applied. Further, reverse current pulses can be applied between the workpiece.

Fig. 6 illustrates a perspective view and Fig. 7 illustrates a cross sectional view of a first anode assembly in accordance with the invention. The anode assembly 500 includes a unique anode-pad arrangement for both plating and polishing the workpiece 802. Multiple strips of pad 502 are attached, glued, or machined onto a cylindrical anode 504 such that the pad 502 protrudes from the outer surface of the anode 504. Electric power is applied to the cylindrical anode 504 and the cathode workpiece 802. As the cylindrical anode 504 rotates about a first axis 510 and the workpiece 802 rotates about a second axis 512, the workpiece 802 is plated when the anode 504 is facing the workpiece (cathode) 802 with no pad in between, and it is polished when the pad 502 is in mechanical contact with the workpiece 802. The workpiece 802 is further adapted to move side to side via workpiece head assembly (not shown), if needed, as indicated by arrow 520. Such unique plating and polishing results from the anode assembly 500 because of the mechanical polishing effects caused by the brushing of the pad 502 against the workpiece surface, and plating of metal from the anode, electrolyte, and workpiece configuration.

Fig. 8 illustrates a perspective view and Fig. 9 illustrates a cross sectional view of a second anode assembly in accordance with the invention. The anode assembly 600 also includes a unique anode-pad arrangement for both plating and polishing the workpiece 802. The anode assembly 600 is formed in a donut or circular shape having a hole 606 in the center. Multiple strips of pad 602 are mounted on the anode 604 such that the pad 602 protrudes from the surface of the anode 604. When electric power is applied to the anode 604 and the cathode workpiece 802, and as the anode 604 rotates about a first axis 610 and the workpiece 802 rotates about a second axis 612, the workpiece 802 is plated when the anode 604 is facing the workpiece 802 with no pad in between, and it is polished when the pad 602 is in mechanical contact with the workpiece 802. As described above, such unique plating and polishing results from the anode assembly 600 because of the mechanical polishing effects caused by the brushing of the pad 602 against the workpiece surface. The diameter or size of the anode assembly 600 may also be smaller than the diameter or size of the workpiece 802.

While operating the anode assemblies in Figs. 6-9, the electrolyte or other solution can be introduced to the mechanical pads 502, 602 from a reservoir (not shown) located in proximity to the anodes 504, 604. In one specific embodiment, the anodes 504, 604 can have an in-channel that includes passageways within the center of anodes 504, 604 and holes that are made in the anode 504, 604, which together provide a path for the solution to be fed to the gap between the anode and the cathode. Alternatively, the electrolyte solution can be dispensed directly onto the anode assemblies

500, 600 through another channel in accordance with the methods described earlier herein.

Additionally, as illustrated in Fig. 7, the electrolyte solution may be contained within a non-conductive chamber 530 that is created around the workpiece. O-rings and other conventional structures, as described earlier herein, may be used to contain the solution within the chamber 530 in this embodiment.

According to the invention, in any of the embodiments, since mechanical action is used to prevent undesired build-up of a conductor on undesired areas of a wafer surface, the need for leveling agents may be reduced, or needed in a smaller percentage than conventionally used.

In a further embodiment, the novel anode assemblies illustrated in Figs. 6-9 can be used to primarily plate/deposit the conductive material on the workpiece surface without polishing the same surface. This is accomplished when the pad or other fixed feature is used only in proximity of the workpiece surface to improve electrolyte mass transfer.

For example, Fig. 10 illustrates a cross sectional view of a "proximity plating" apparatus and method in accordance with the present invention. Fig. 10 illustrates a nonconductive chamber 700 having the electrolyte solution 11 disposed therein. The chamber 700 includes the anode assembly 500 having multiple strips of pad 502 or fixed features mounted, or machined onto the cylindrical anode 504. During operation, when the pad strips 502 are rotating about axis 510 and are spaced apart from the workpiece 802 (the pad strips 502 do not make direct contact with the workpiece 802), the workpiece 802 is plated using the electrolyte solution 11. The anode 510 and pad strips 502 should preferably rotate at a rate such that the electrolyte solution 11 is continuous and is applied/splashed to the workpiece 802, and thus forming a closed electrical circuit through the anode assembly 500, electrolyte, and the workpiece (cathode) 802. When a gap 800 is about 0-5 mm and contains a meniscus solution of electrolyte, a very high mass transport results, thereby depositing high quality metal films onto the workpiece surface. Moreover, depending on the type, shape, and structure of the pad or the fixed feature attached to the cylindrical anode 504, the gap 800 may be greater than 5 mm.

In the embodiments described herein, the hardness of the pad or fixture is coupled with the relative speed of travel of the pad to the workpiece. Preferably, the pad should be porous and hard for optimal performance.

The present invention may reduce the need for pulse generating power supplies because the mechanical pulsing that is generated from the movement of the pad relative to the face of the workpiece creates sufficient pulsing. This mechanical pulsing is created as a result of the wafer being in proximity with the pad as it is moved in relation to the workpiece. The benefit of the mechanical pulsing is that it improves grain size, filling efficiency of the contact holes, vias, and trenches, and copper film integrity without the need for power supplies with pulsing capabilities.

Figs. 11 and 12A-12B will now be used to describe an improved embodiment of the invention. It has been determined that the present invention can also advantageously affect the texture of a conductive material that has been applied using a plating process. Fig. 11 illustrates a conventional substrate 900, having deposited thereon a barrier layer 902 and an epitaxial seed layer 904. As illustrated, the seed layer 904 is composed of individual grains 906, which are oriented in a predetermined manner, such as a <111> crystal orientation. After a conventional plating process, the atoms that make up the conductive plating layer 908 applied thereto will, over time, cluster to form grains 910, which grains 910 retain the original crystal orientation of the seed layer 904 disposed below. Accordingly, if the seed layer 904 has a <111> crystal orientation, so will the conductive plating layer 908.

In contrast, the invention has found that by plating and polishing, as described above, the polishing changes the crystal orientation of the applied conductive plating layer to become more random. As shown in Fig 12A, upon the application of a first level 958A of atoms in the plating layer 958, the polisher, such as pad 402 previously described, polishes the first level of atoms and causes dangling bonds in the atoms at that first level. Thus, as shown in Fig. 12B, the next level of atoms applied thereover will not form in the same manner as the first level was formed. It has been determined that the action of polishing causes atoms to form in a manner such that, over time, the grains that naturally form as the atoms cluster tend to have a different texture than they would otherwise have. Typically, this texture manifests itself as being more random. This is shown in Fig. 12B as grains 960 that result. Thus, the plating layer 958 will not have the same crystal orientation as the seed layer.

As the process is repeated, and plating continues and the applied grains are polished, this leads to a plating layer 968 having a greater degree of randomness at the grain level, and, accordingly, a plating layer have more uniform characteristics.

It has been determined that the first few layers of atoms applied over the seed layer 904 can be polished and this will effectively change the resultant grain pattern. It is also possible to continue to polish the atoms applied throughout the plating process, thus continuing to increase this effect.

Although only the above embodiments have been described in detail above, those skilled in the art will readily appreciate that many modifications of the exemplary embodiment are possible without materially departing from the novel teachings and advantages of this invention.

Claims

I claim:

1. An apparatus for plating and polishing a surface of a semiconductor workpiece, comprising:

a first chamber having a plating device for plating the surface of the workpiece;

a second chamber having a polishing device for polishing the surface of the workpiece; and

a partition separating the first chamber from the second chamber.

2. The apparatus according to claim 1, wherein the plating device comprises a pad mounted on a cylindrical anode.

3. The apparatus according to claim 2, wherein the cylindrical anode is adapted to rotate about a first axis.

4. The apparatus according to claim 1, wherein the plating device comprises an anode plate mounted in proximity to a bottom side of the first chamber.

5. The apparatus according to claim 1, wherein the polishing device comprises a pad mounted on a cylindrical anode.

6. The apparatus according to claim 5, wherein the cylindrical anode is adapted to rotate about a first axis.

7. The apparatus according to claim 1, wherein the polishing device comprises a chemical mechanical polishing device.

8. The apparatus according to claim 7, wherein the chemical mechanical polishing device comprises a pad mounted on a cylindrical roller.

9. The apparatus according to claim 8, wherein the cylindrical roller is adapted to rotate about a first axis.

10. The apparatus according to claim 1 further comprising an electrolyte solution disposed in the first and second chambers.

11. The apparatus according to claim 1 further comprising a workpiece support adapted to support the workpiece during plating and polishing, wherein the workpiece support is adapted to rotate about a second axis and adapted to move from side to side.

12. The apparatus according to claim 1, wherein the workpiece comprises one of a wafer, a flat panel, and a magnetic film head.

13. A method of plating and polishing a surface of a semiconductor workpiece, the method comprising the steps of:

plating a conductive material to the surface of the workpiece using an electrolyte solution disposed on the surface of the workpiece, the workpiece being disposed in proximity to an anode; and

polishing the surface of the workpiece during at least certain of the times when the plating is not being performed.

14. A method according to claim 13, wherein the plating step is performed in a first chamber and the polishing step is performed in a second chamber.

15. A method according to claim 14, wherein the first chamber and the second chamber are separated by a partition.

16. A method according to claim 13, wherein the plating step is performed using one of a brush plating and an electrochemical mechanical deposition.

17. A method according to claim 13, wherein the polishing step is performed using one of an electropolishing and a chemical mechanical polishing.

18. A method according to claim 13, wherein the plating step is performed before the polishing step.

19. A method according to claim 13, wherein the workpiece comprises one of a wafer, a flat panel, and a magnetic film head.

20. A pad assembly for plating and polishing a semiconductor workpiece, comprising:

a cylindrical anode having an outer surface; and

a plurality of pad strips mounted on the cylindrical anode such that the plurality of pad strips protrude from the outer surface of the cylindrical anode.

21. The pad assembly according to claim 20, wherein the cylindrical anode is adapted to rotate about a first axis.

22. The pad assembly according to claim 20, wherein plating is performed when the pad strips are not in contact with the workpiece, and polishing is performed when the pad strips are in contact with the workpiece.

23. The pad assembly according to claim 20, wherein the workpiece comprises one of a wafer, a flat panel, and a magnetic film head.

24. A pad assembly for plating and polishing a semiconductor workpiece, comprising:

a circular or donut shaped anode having a top surface; and

a plurality of pad strips mounted on the top surface of the anode such that the plurality of pad strips protrude from the top surface of the anode.

25. The pad assembly according to claim 24, wherein the anode is adapted to rotate about a first axis.

26. The pad assembly according to claim 24, wherein plating is performed when the pad strips are not in contact with the workpiece, and polishing is performed when the pad strips are in contact with the workpiece.

27. The pad assembly according to claim 24, wherein the workpiece comprises one of a wafer, a flat panel, and a magnetic film head.

28. A method of depositing a conductive material from an electrolyte solution to a

predetermined area of a workpiece comprising the steps of:

intermittently applying the conductive material to the workpiece using the electrolyte solution disposed on a surface of the workpiece, the workpiece being disposed in proximity to an anode; and

polishing the workpiece during at least certain of the times when the intermittent application is not being performed.

29. A method according to claim 28, wherein the workpiece comprises one of a wafer, a flat panel, and a magnetic film.

30. An anode assembly for plating a semiconductor workpiece, comprising:

an anode having an outer surface; and

a plurality of pad strips or fixed features attached on the anode such that the plurality of pad strips protrude from the outer surface of the anode.

31. The pad assembly according to claim 30, wherein the anode is adapted to rotate about a first axis.

32. The pad assembly according to claim 30, wherein plating is performed when the pad strips or fixed features are in proximity to the workpiece.

33. The pad assembly according to claim 32, wherein the pad strips or fixed features are within 0-5 mm from the workpiece.

34. A method of plating a conductive material from an electrolyte solution to a surface of a workpiece comprising the steps of:

continuously applying the electrolyte solution on the surface of the workpiece, the electrolyte solution being applied to the surface using an anode rotating about a first axis while generating a closed electrical circuit between the anode and the workpiece; and

providing an electric potential between the anode and the workpiece.

35. A method according to claim 34, wherein the anode includes an outer surface having a plurality of pad strips or fixed features attached thereon.

36. A method according to claim 35, wherein the continuously applying step further includes the step of splashing or agitating the electrolyte solution near the surface using the plurality of pad strips or fixed features.

37. A method according to claim 35, wherein the plurality of pad strips or fixed features are in close proximity to the surface of the workpiece.

38. A method of depositing a conductive material from an electrolyte solution to a predetermined area of a workpiece containing a seed layer disposed thereon comprising the steps of:

applying said conductive material over said seed layer of said workpiece using said electrolyte solution disposed on a surface of said workpiece, said workpiece being disposed in proximity to an anode; and

mechanically polishing said workpiece during at least certain of the times when said application is being performed, thereby altering the texture of the conductive material being applied

39. A method according to claim 38, wherein the texture of the conductive material being applied becomes more random.

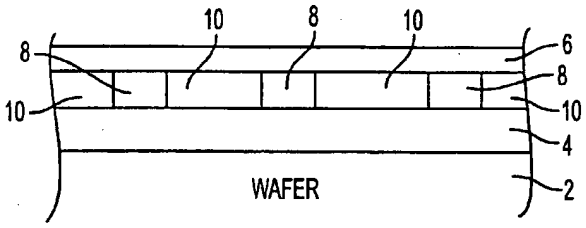
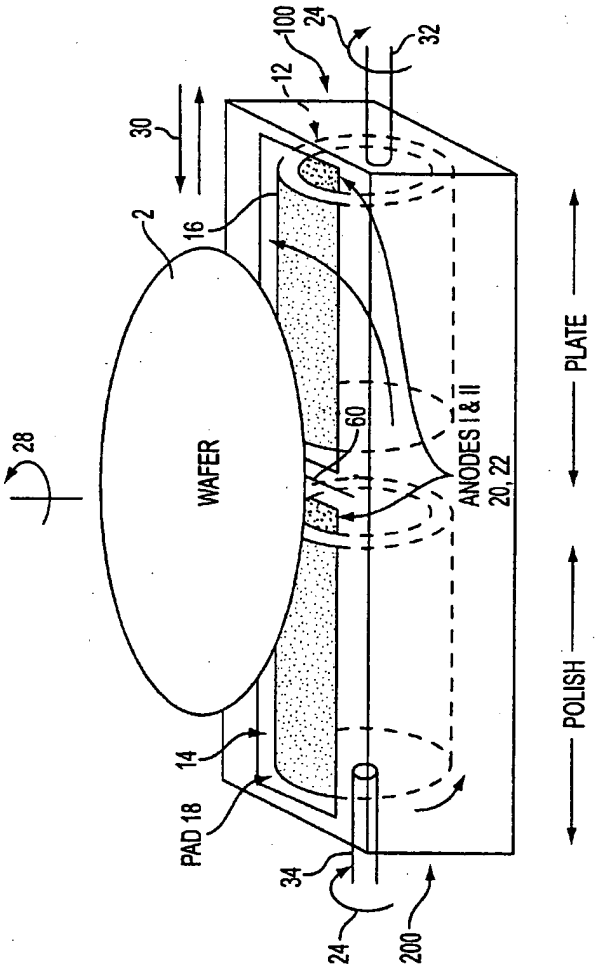


FIG. 1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12
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PLATE
POLISH
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PAD 18
34
24
200

FIG. 2

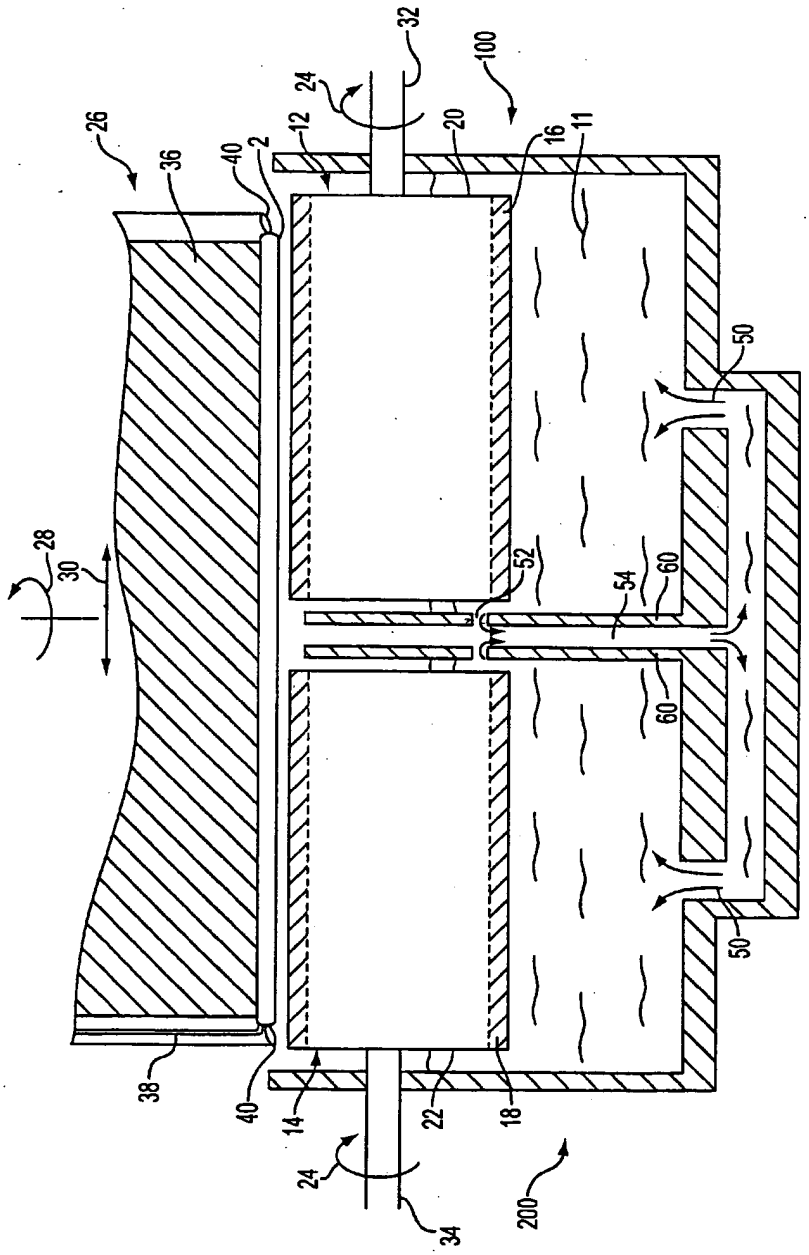
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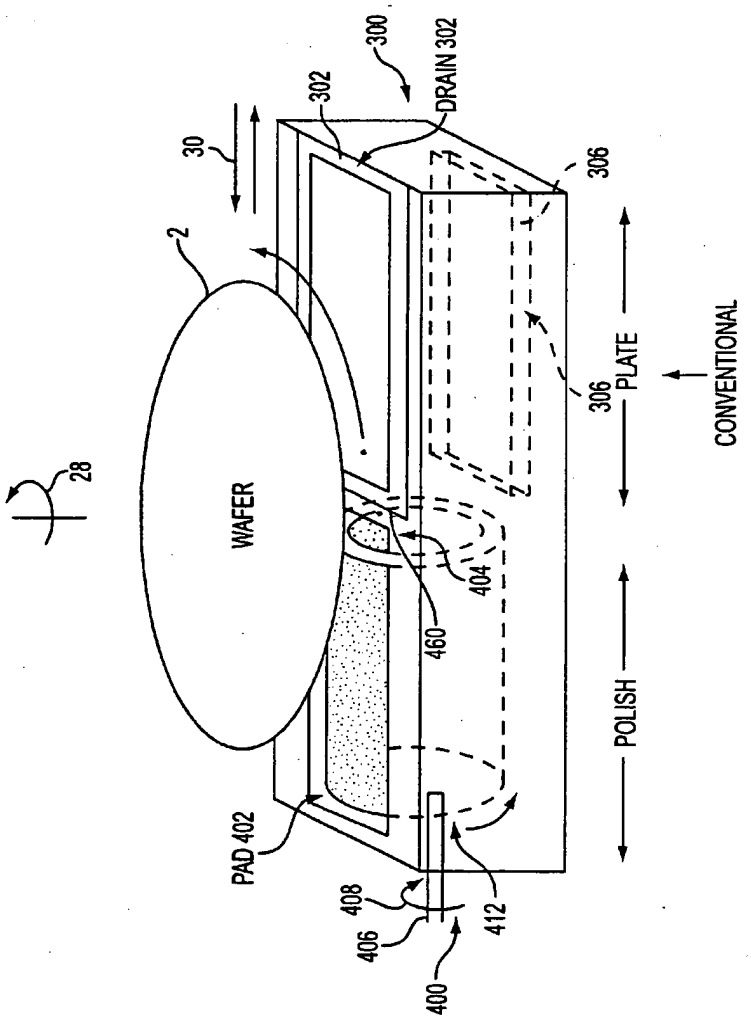
PLATE
POLISH

FIG. 3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412
400

FIG. 4

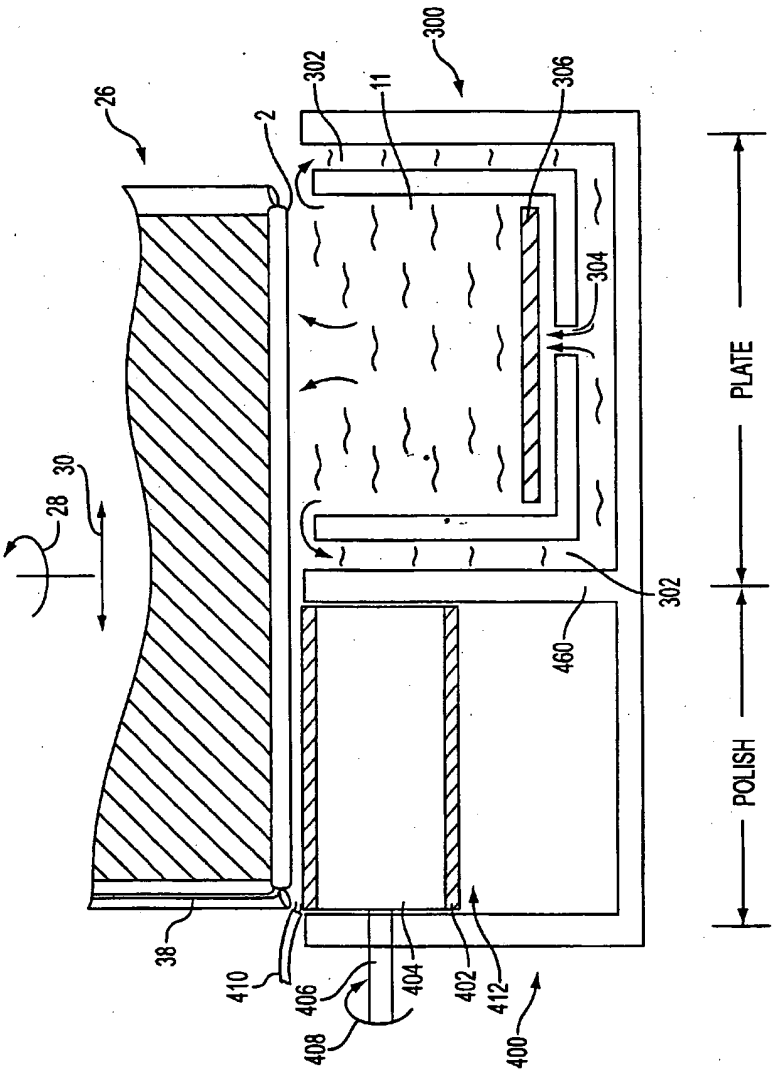
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FIG. 5

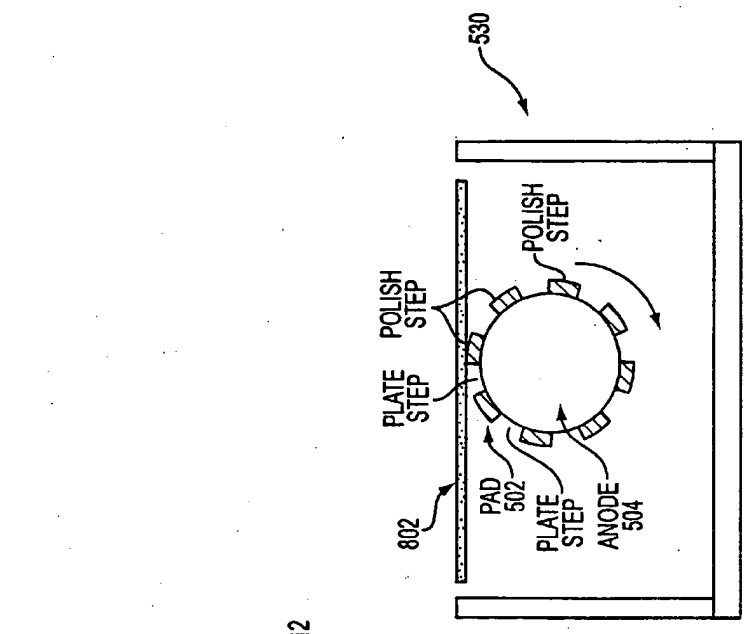
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PLATE STEP
802
PAD 502
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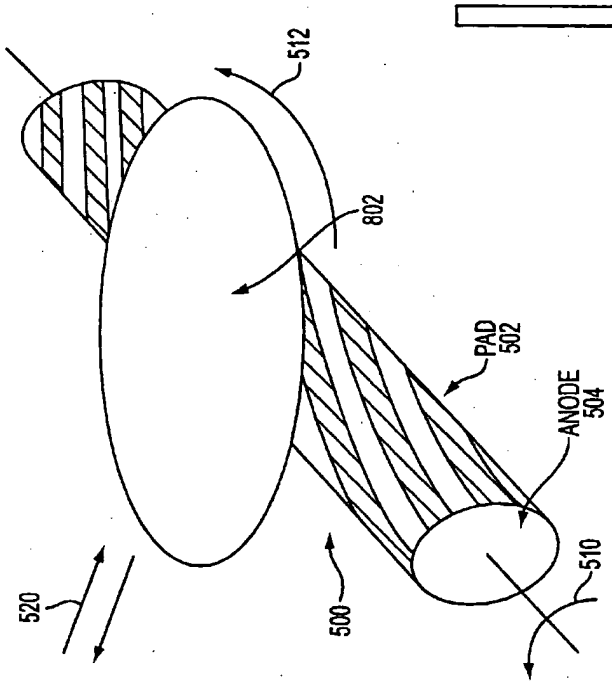
ANODE 504

FIG. 7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ANODE 504
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500

FIG. 6

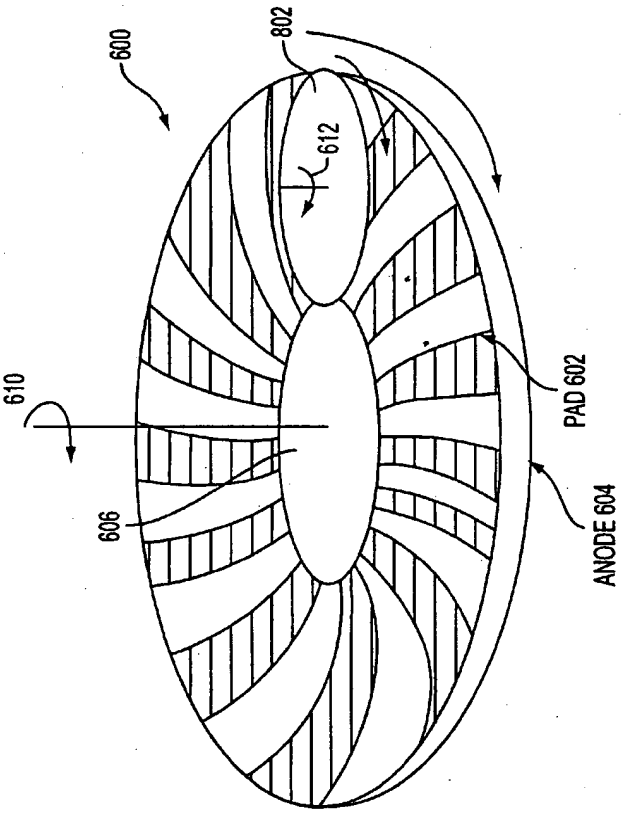

FIG. 8

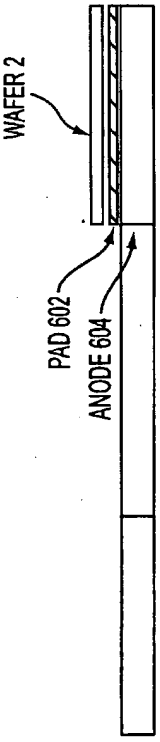

FIG. 9

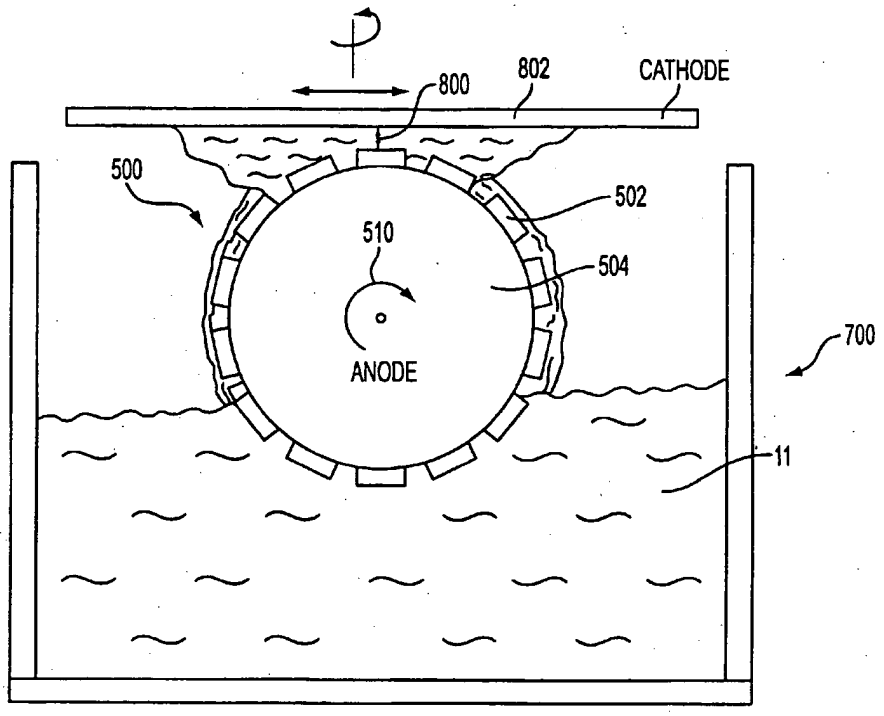

FIG. 10

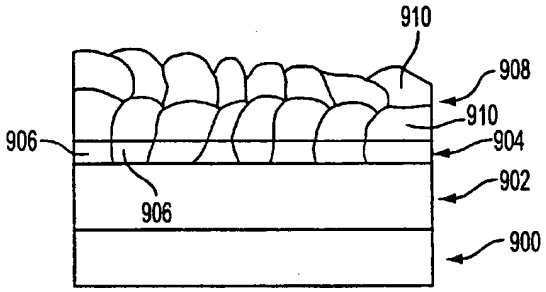

FIG. 11

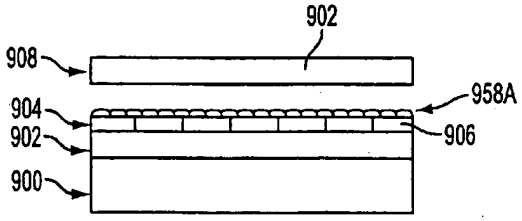

FIG. 12A

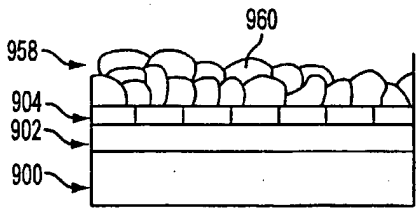

FIG. 12B

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 00/08336

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 B24B37/04 B24B41/047 B24B41/00 B24D13/06 B24D13/14
H01L21/288 H01L21/321

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B24B B24D H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 903 774 A (EBARA CORP) 24 March 1999 (1999-03-24) column 3, line 43 -column 4, line 37	1,7, 13-19, 28,29
X	US 3 890 746 A (SAEGUSA KYUJI ET AL) 24 June 1975 (1975-06-24) column 4, line 35 - line 47; figure 3	20,21, 30,31
P,X	EP 0 960 693 A (SPEEDFAM CO LTD) 1 December 1999 (1999-12-01) abstract; figure 2	24,25
A	US 3 395 092 A (RIBES VINCENT) 30 July 1968 (1968-07-30) the whole document	22,26, 32,34,38

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 July 2000	01/08/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Petrucci, L

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INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 00/08336

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	WO 95 00295 A (MINNESOTA MINING & MFG) 5 January 1995 (1995-01-05) abstract; figures 3,4	24,25
A	US 3 436 259 A (REGH JOSEPH ET AL) 1 April 1969 (1969-04-01) the whole document	

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte. onal Application No
PCT/US 00/08336

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0903774 A	24-03-1999	JP 11315383 A	16-11-1999
		JP 11154653 A	08-06-1999
		WO 9945170 A	10-09-1999
US 3890746 A	24-06-1975	JP 822931 C	28-07-1976
		JP 50039871 B	19-12-1975
		JP 50050787 A	07-05-1975
		DE 2430522 A	20-03-1975
		FR 2243053 A	04-04-1975
		GB 1456693 A	24-11-1976
EP 0960693 A	01-12-1999	JP 11333703 A	07-12-1999
US 3395092 A	30-07-1968	NONE	
WO 9500295 A	05-01-1995	DE 69406446 D	27-11-1997
		DE 69406446 T	28-05-1998
		EP 0702615 A	27-03-1996
		ES 2109709 T	16-01-1998
		JP 8511733 T	10-12-1996
US 3436259 A	01-04-1969	DE 1621473 A	23-07-1970
		FR 1517308 A	12-07-1968
		GB 1168536 A	29-10-1969